What is claimed is:

1. A display driver comprising:

a memory area which has a storage capacity for storing an amount of image data that is enough to display a single screen, each image data being composed of a plurality of bits; and

a memory control circuit for storing, in a first mode, a whole of the image data of the plurality of bits into the memory area and for storing, in a second mode, a part of the image data of the plurality of bits into the memory area to leave an empty area in the memory area.

2. A display driver as claimed in claim 1, wherein the part of the image data formed by the plurality of bits is a predetermined number of high order bits within a plurality of bits representative of the number of gradation levels.

3. A display driver as claimed in claim 2, wherein the memory area is divided into a plurality of subdivided memory areas that are equal in number to the bit number providing the gradation levels of the image data given by the plurality of bits;

in the first mode, the image data being divided at every one bit for the plurality of bits corresponding to the number of the gradation levels and the whole of the image data divided at every one bit being stored in the plurality of the subdivided memory areas;

in the second mode, the highest order bit of the plurality of bits forming the number of the gradation levels in the image data being stored as the part of the image data into a selected one of the subdivided memory areas.

4. A display driver as claimed in claim 3, wherein, in the second mode, a display screen is driven on or off by a binary drive operation, corresponding to the image data stored in the selected one of the subdivided memory areas.

5. A display driver as claimed in claim 1, wherein, in the second mode, image data different from the above-mentioned image data of the plurality of bits is input and desired high order bit or bits within the number of the gradation levels

of the different image data are stored in the empty area in the memory area.

6. A display driver as claimed in claim 5, wherein the image data different from the above-mentioned image data is specified by image data that is next to a current screen in consecutive screens or image data that is obtained by subjecting, to predetermined processing, the image data stored in the memory area as a part of the image data formed by the plurality of bits.

7. A display driver as claimed in claim 1, wherein, in the second mode, the image data of the plurality of bits converted into a prescribed number of bits and subjected to a color decrease process is input;

the image data of the plurality of bits converted into the prescribed number of bits and subjected to the color decrease process being used as the part of the image data formed by the plurality of bits.

8. A display driver as claimed in claim 7, wherein, in the second mode, the image data of the plurality of bits converted into the prescribed number of bits and subjected to the color decrease process are input in parallel with image data of a plurality of bits obtained by converting different image data into a desired number of bits and subjecting the same to a color decrease process.

9. A display driver as claimed in claim 8, comprising:

in the second mode, a color decrease circuit for converting input image data of a plurality of bits into the prescribed number of bits and subjecting the color decrease process, to produce the color decreased bits as the part of the plurality of bits.

10. A display driver as claimed in claim 9, wherein the color decrease circuit is structured by a dither circuit for carrying out a dither process.

11. A display driver as claimed in claim 1, comprising:

in the second mode, a processing circuit for subjecting, to a predetermined process, input image data of the plurality of bits or for subjecting, to the predetermined process, image data given from color decrease circuit, to output the part of the plurality of bits.

12. A display driver as claimed in claim 1, comprising:

in the second mode, a processing circuit for storing the image data of the plurality of bits input as the part of the plurality of bits stored in the memory area, into the empty area or for storing the image data that is output from the color decrease circuit and that is subjected to the predetermined process, into the empty area as the part of the plurality of bits.

13. A display driver as claimed in claim 1, wherein the memory area is divided into a plurality of subdivided memory areas by a division number;

in the first mode, the image data formed by the plurality of bits being divided into a desired number of bits by a number corresponding to the division number and the whole of the image data divided into the desired number of bits is stored in the plurality of the subdivided memory areas;

in the second mode, either one of the subdivided memory areas being selected to store the part of the image data formed by the plurality of bits.

14. A display driver as claimed in claim 1, wherein the memory area is divided into a first divided memory area and a second divided memory area;

in the first mode,

the image data formed by the plurality of bits being equally divided in the first mode into high and low order bits for a plurality of bits representative of the number of gradation levels;

the high order bits of the image data among the plurality of bits divided being stored in the first divided memory area while the low order bits of the image data of the image data among the plurality of bits divided are stored in the second divided memory area;

in the second mode,

the high order bits of the image data formed by the plurality of bits being used as the part of the image data formed by the plurality of bits and selectively stored in the first divided memory area or the second divided memory area.

15. A display driver as claimed in claim 1, wherein, in the case of

controlling two display screens, in the first mode, the memory control circuit uses the whole of the plurality of bits stored in the memory area to display on either one of the two display screens;

in the second mode, the memory control circuit using the part of the plurality of bits stored in the memory area to display on at least one of the display screens.

16. A display driver as claimed in claim 1, wherein, in the first mode, the memory control circuit reads out the whole of the image data stored in divided memory areas as image data used for displaying;

in the second mode, the memory control circuit reading out the image data stored in either one of the divided memory areas as high order bits of the image data used for displaying and, in addition, using the same data as the readout data, the part of the readout data, or predetermined desired data as low order bits of the image data used for displaying.

17. A display driver as claimed in claim 1, comprising:

a first judgment circuit for controlling the first and the second modes by comparing the input image data of the plurality of bits with the memory capacity of the memory area.

18. A display driver as claimed in claim 17, comprising:

a second judgment circuit for controlling the first and the second modes by judging whether or not the input image data of the plurality of bits are subjected to a predetermined process.

19. A display driver as claimed in claim 1, wherein the first and the second modes are controlled by a mode selection signal given from an external circuit.

20. A display driver as claimed in claim 1, wherein, in the second mode, the memory control circuit controls a bit width of the part of the plurality of bits in response to a bit number selection signal.